MODULES WITH BUILT-IN DATA RAM

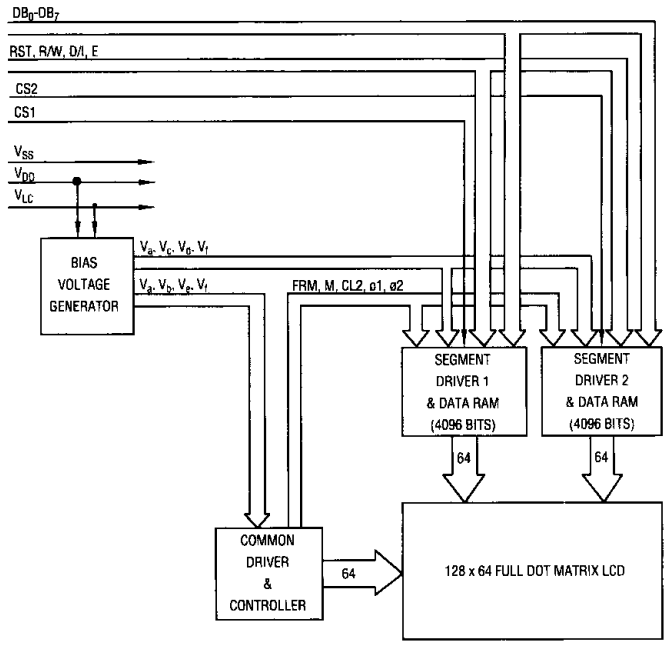
The **Seiko Instruments** liquid crystal display modules G1213 and G1216 are used to upgrade character-only modules in an easy and cost-effective way.

These compact graphic LCD modules can be used in personal translators, medical and scientific instrumentation, data collection, telephones, pagers, and any other devices that you can imagine. The new series of compact graphic LCD modules, G1213 and G1216 have the following features:

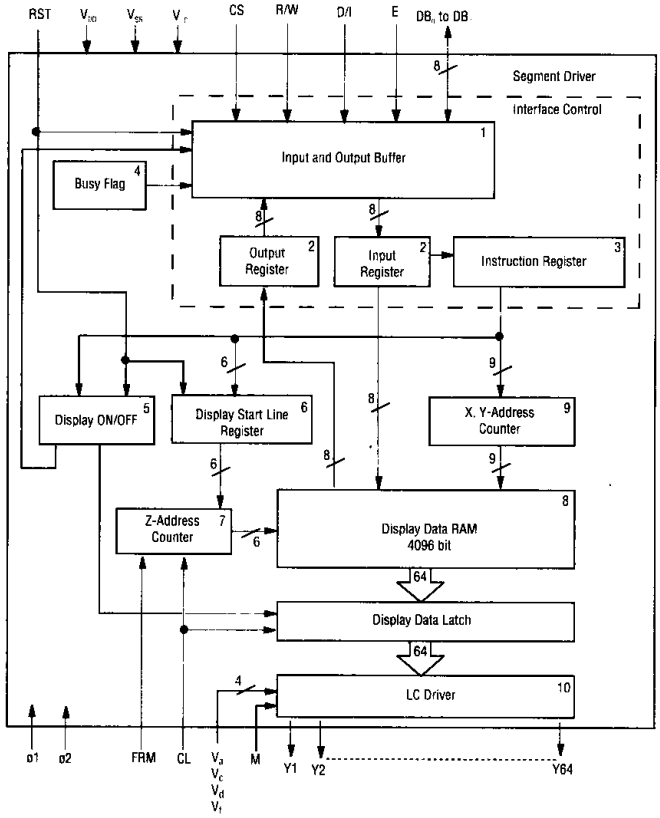
- ▶ 128 x 32 and 128 x 64
- ▶ Wide operating temperature range (-20°C to +70°C)
- ▶ High contrast for easy viewing
- ▶ STN reflective or optional LED backlight version
- ▶ Built-in RAM that eliminates external controllers
- ▶ Lower power consumption (+5V @ 2.0 mA and -8V @ 1.8 mA)

CIRCUIT BLOCK DIAGRAM (G1213, G1216)

The following block diagram shows the basic operation of the G1216. Model G1213 is similar with only one segment driver and 4096 bits of data RAM.



SEGMENT DRIVER & DATA RAM DETAILED BLOCK DIAGRAM (G1213, G1216)



FUNCTIONS AND OPERATIONS OF MAIN BLOCKS (G1213, G1216)

INTERFACE CONTROL UNIT

The interface control unit consists of the following blocks:

1) Input and output buffer
2) Input and output register
3) Instruction register

The above blocks are selected according to the following combinations of R/W and D/I signals:

R/W	D/I	Functions
1	1	Output Register Read Internal Operation (Display Data RAM → Output Register)
O	1	Input Register Write Internal Operation (Input Register → Display Data RAM)
1	O	Busy Check and Status Read
O	O	Instruction Write

1) INPUT AND OUTPUT BUFFER

The data is transmitted through eight data buses (DB0 to DB7).

DB7 MSB (most significant bit)
DB0 LSB (least significant bit)

The data can input and output only when the Chip Select is selected. Therefore, if the Chip Select is not selected, the internal condition remains unchanged and instruction will not be executed, even when changing the signal of the input terminals excluding the RST (reset) terminal.

Note that the RST operates regardless of CS1 and CS2.

2) INPUT AND OUTPUT REGISTER

This product is provided with an input register and an output register so that the product can interface with MPUs having speed differing from the internal operation.

INPUT REGISTER

The input register is a register that is used for temporarily storing the data to be written in the display data RAM. The data to be written from the MPU to the input register will be automatically written in the display data RAM through internal operation.

When the Chip Select is selected and R/W = 0, D/I = 0, the data is written in the register, synchronized with the fall of signal E.

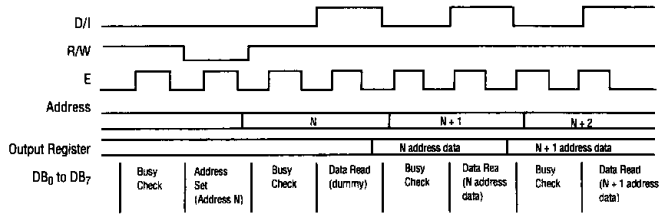
OUTPUT REGISTER

The output register is a register that is used for temporarily storing the data to be read from the display data RAM.

3) INSTRUCTION REGISTER

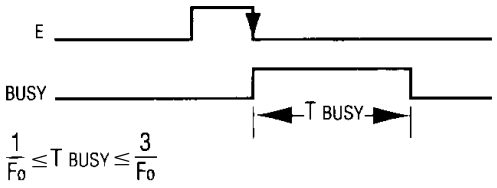
In order to read the content of the output register, the Chip Select must be selected, D/I must be 1, and R/W must be 1. When executing the Read instruction, the contents of the output register stored at that time are output during the time that “E” is 1. When “E” falls, display data of currently indicated address is written in the output register. After that, the address advances by one.

The contents of the output register are rewritten by the Read instruction. The data is retained by the address set or other instructions. Accordingly, when performing the address set, and next executing the Read instruction, the data of the specified address is not output and the data of the address which is specified is output at the second data read time. Therefore, when setting the address, a dummy read is needed once.



4) BUSY FLAG

The status when busy flag is “1” means that the module is operating internally. Instructions other than the Status Read are not available at this time. The busy flag is output to DB7 by the Status Read instruction. Ensure that the busy flag is “0” before executing the instruction.



F∅ is frequency of ∅1 or ∅2
(1/2 the source oscillation frequency of HD61203): 215 KHz typ.)

5) DISPLAY ON/OFF FLIP/FLOP

The display ON/OFF Flip/Flop is a flip-flop function that determines whether the display data corresponding to the RAM data is output to the segment on the LCD (ON status) or goes to all nonlit status regardless of the RAM data (OFF status). This is controlled by the display ON/OFF instruction. When the RST signal becomes "0", the display goes to OFF status. This flip-flop status is output to DB5 by the Status Read instruction.

Even when performing display ON/OFF, the data inside the RAM is not affected.

6) DISPLAY START LINE REGISTER

The display start line register is a register that determines the line address for which data is displayed on the top line of the LCD screen when displaying the contents of the display data RAM on the LCD screen. It is also used to scroll the display. The 6-bit (0 to 63) display start line information is written in this register by the Display Start Line Set instruction.

The contents of this register are transmitted to address counter Z at "H" level of the FRM signal (common driver output) which indicates the display start on the screen.

7) Z-ADDRESS COUNTER

The Z-address counter generates the address to output the display data synchronized with the common signal. This is a 6-bit counter which counts at the fall of the CL signal (common driver output). The contents of the display start line register are preset to the Z-address counter at "H" level of the FRM signal (common driver output).

8) DISPLAY DATA RAM

The display data RAM is a RAM that stores the display dot data. 1 bit of RAM data corresponds to lighting (data =1) or non-lighting (data = 0) of 1 dot of the display on the LCD screen.

9) X,Y-ADDRESS COUNTER

X,Y-address counter is a 9-bit counter which gives the address of the internal display data RAM. It is necessary to set the X-address counter of the three upper bits, and the Y-address counter of the six lower bits using differing instructions.

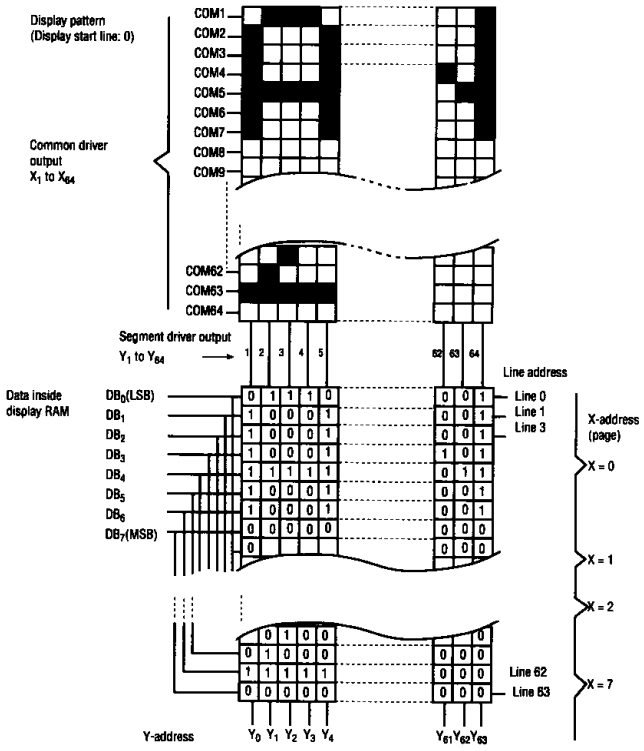
X-ADDRESS COUNTER

Address counter X is a simple register that is not provided with a count function. The address is set by instruction.

Y-ADDRESS COUNTER

This counter sets the address by instruction and is automatically advanced by the read/write operation. Counting is performed by looping the values 0 to 63.

RELATIONSHIP BETWEEN DISPLAY AND DATA INSIDE DISPLAY RAM

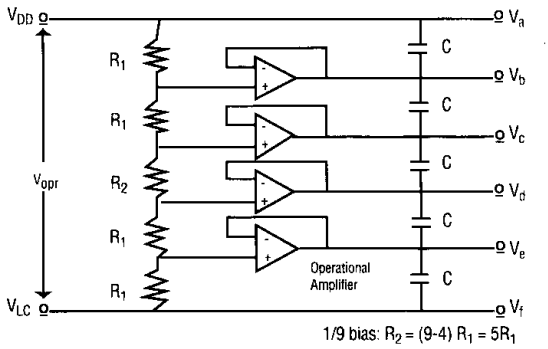


10) COMMON DRIVER (HD61203)

The common driver is a 64-drive output CMOS IC. Incorporating an oscillation circuit, this driver generates the common signal and timing signals (LC AC drive control, and one-frame timing signal) necessary for the LC display, and controls the display by supplying the timing signals to the segment drivers.

11) BIAS VOLTAGE GENERATOR

Six levels of standard voltage V_a to V_f are applied to the drivers as a bias voltage. This voltage is generated by resistance division of Vopr and driven by a voltage follower through an operational amplifier.



SOFTWARE INSTRUCTIONS (G1213, G1216)

Instructions other than the Status Read instruction will not be executed if they are sent while another instruction is already being executed. The busy flag is "1" when executing the instruction. Check whether or not the flag is "1" before transmitting the instructions from the MPU.

		CODE										
	Instruction	R/W	D/1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
1	Display ON/OFF	0	0	O	O	1	1	1	1	1	1/0	Turns ON/OFF total display. Date and internal status in the display RAM remain unchanged. 1:ON O:OFF
2	Display start line	0	0	1	1	Display start lines (0 to 63)						Determines the RAM line to be displayed on the top line (COM1) on the display.
3	X-address (page) set	0	O	1	O	1	1	1	X-address (page) (0 to 7)			Sets the X-address of the RAM (page) in the X-address (page) register.
4	Y-address set	O	0	O	1	Y-address (0 to 63)						Set Y-address of the RAM in the Y-address counter.
5	Status read	1	O	BUSY	0	ON/OFF	RESET	0	O	0	0	Reads the status. RESET 1:Reset 0:Normal ON/OFF 1:Display OFF, 0:Display ON BUSY: 1:During internal operation 0:READY status
6	Display data write	O	1	Write data								Writes data to DB0 (LSB) to DB7 (MSB) on the data bus into the display RAM. Accesses the RAM in which address has been specified beforehand. After that the Y-address advances by one.
7	Display data read	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM into the data bus.

Note: The BUSY time varies depending upon the frequency FØ (:215 kHz (typ.)) of Ø1, Ø2 ($1/F\emptyset \leq T_{BUSY} \leq 3/F\emptyset$).

1) DISPLAY ON / OFF (G1213, G1216)

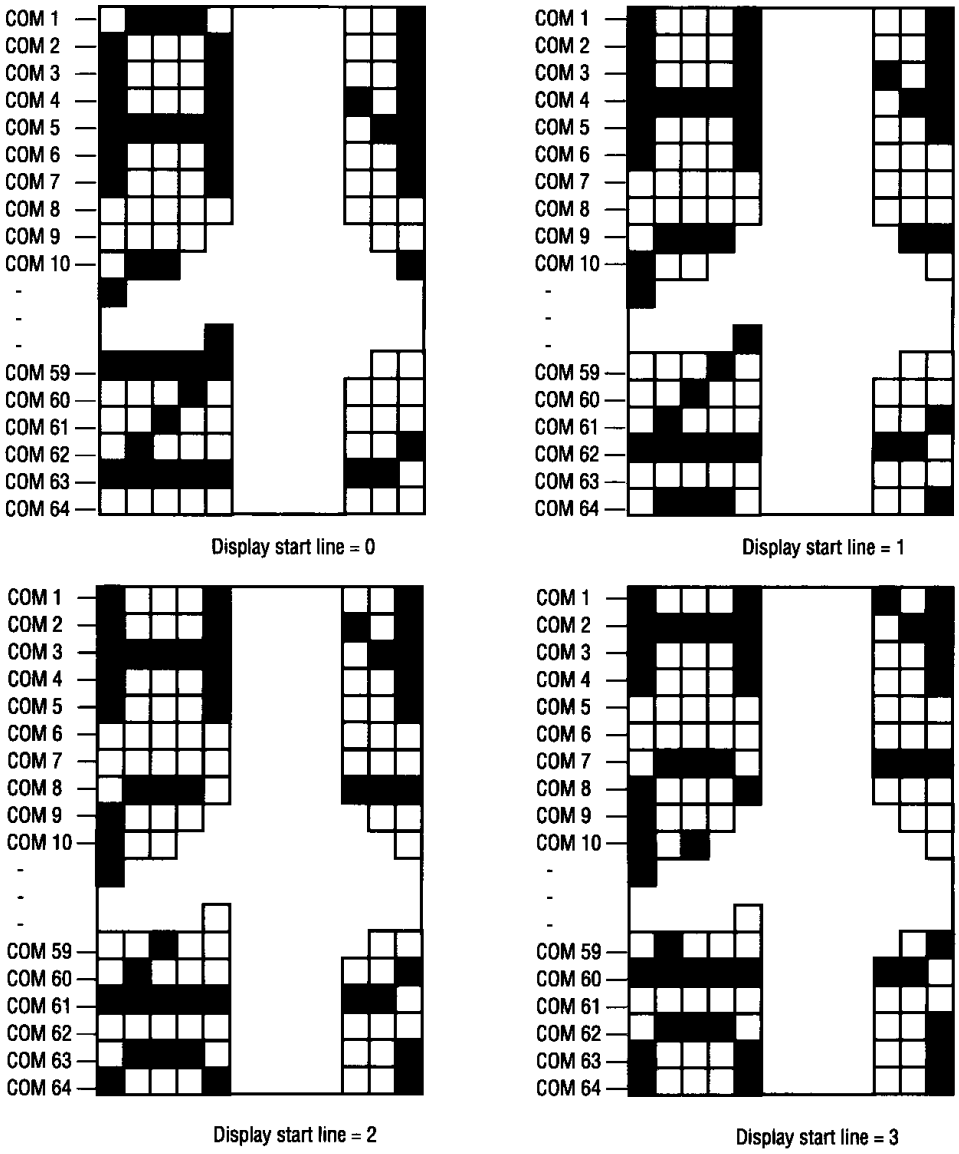
	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

Turns the display ON when D = 1, and OFF when D = 0. When the display is turned OFF by D = 0, the original display appears if D is set to 1 because the display data is retained in the display data RAM.

2) DISPLAY START LINE (G1213, G1216)

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A
				← Upper bits					Lower bits →	

Sets the display data RAM line address expressed with binary AAAAAA in the display start line register. When displaying the content of the display data RAM, the display data on the line addresses which are set in the register are displayed on the top line on the LCD screen.



Relationship Between Display Start Lines and Displays

3) X-ADDRESS (PAGE) SET (G1213, G1216)

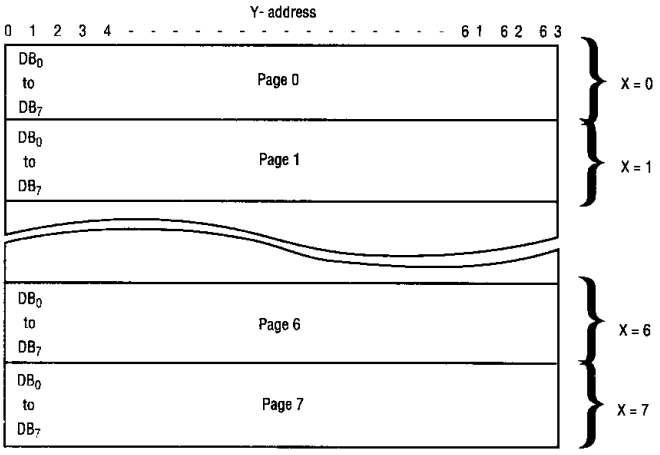
	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A
				← Upper bit					Lower bit →	

The display data RAM “X” address (page) which is expressed with binary AAA is set in the X-address register. Following write/read operations from the MPU are performed on the specified X-address (page) until the next X-address (page) set is performed.

4) Y-ADDRESS SET (G1213, G1216)

	R/W	D/I	DB7								DB0
Code	0	0	0	1	A	A	A	A	A	A	
				← Upper bit						Lower bit →	

The display data RAM Y-address which is expressed with binary AAAAAA is set in the Y-address counter. After that the Y-address counter advances by one each time write/read is performed from the MPU.



Display Data RAM Address Configuration

5) STATUS READ (G1213, G1216)

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/OFF	RESET	0	0	0	0
			← Upper bits							Lower bits →

BUSY: When BUSY = 1, it means that the module is operating internally and the next instruction is not accepted until BUSY = 0. After confirming that BUSY = 0, it is necessary to perform the next write.

ON/OFF: Indicates that the display is OFF when ON/OFF = 1. Indicates that the display is ON when ON/OFF = 0.

RESET: Indicates that initial setup is performed by the RST signal.

Indicates that the initialization is being performed when RESET = 1 and instructions other than the Status Read instruction are not accepted.

(6) DISPLAY DATA WRITE (G1213, G1216)

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D
			← Upper bit							Lower bit →

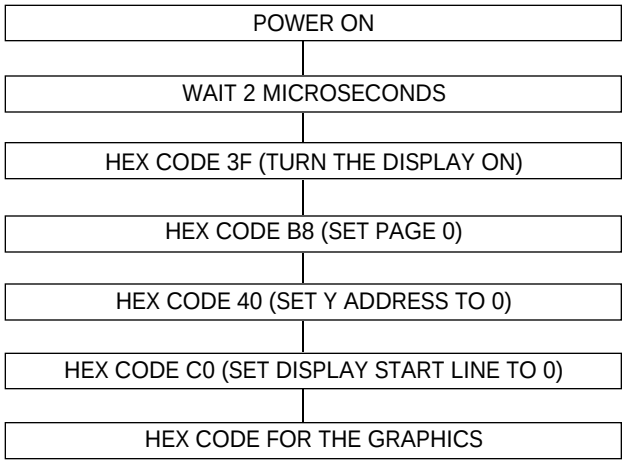
Writes 8-bit binary data DDDDDDDD in the display data RAM. After the write is completed, the Y-address is automatically advanced by one.

7) DISPLAY DATA READ (G1213, G1216)

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D
			← Upper bit							Lower bit →

Read 8-bit binary data DDDDDDDD from the display data RAM. After read is performed, the Y-address is automatically advanced by one. A dummy read is necessary once, immediately after the address set is completed.

SAMPLE SOFTWARE INSTRUCTION (G1213, G1216)

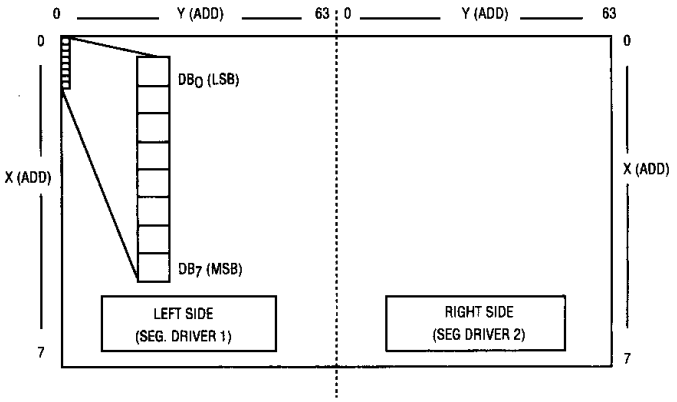


MODULES WITH BUILT-IN DATA RAM

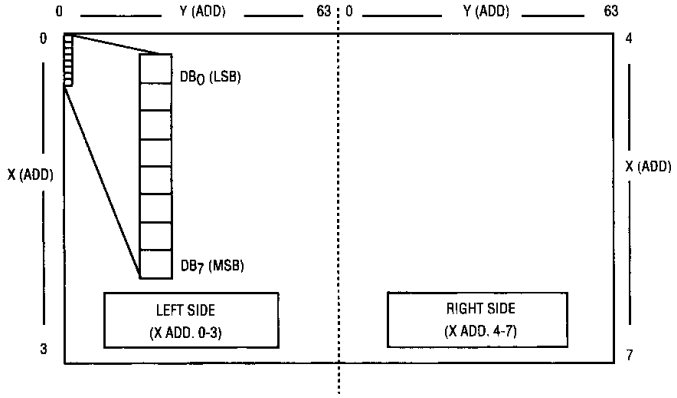
HEXADECIMAL CODE FOR CHARACTERS (8 BYTES PER CHARACTER)

Text 0:	Byte	3EH, 7FH, 71H, 59H, 4DH, 7FH, 3EH, OOH
Text 1:	Byte	40H, 42H, 7FH, 7FH, 40H, 40H, OOH, OOH
Text 2:	Byte	62H, 73H, 59H, 49H, 6FH, 66H, OOH, OOH
Text 3:	Byte	22H, 63H, 49H, 49H, 7FH, 36H, OOH, OOH
Text 4:	Byte	18H, 1CH, 16H, 53H, 7FH, 7FH, 50H, OOH
Text 5:	Byte	27H, 67H, 45H, 45H, 7DH, 39H, OOH, OOH
Text 6:	Byte	3CH, 7EH, 4BH, 49H, 79H, 30H, OOH, OOH
Text 7:	Byte	03H, 03H, 71H, 79H, OFH, 07H, OOH, OOH
Text 8:	Byte	36H, 7FH, 49H, 49H, 7FH, 36H, OOH, OOH
Text 9:	Byte	06H, 4FH, 49H, 69H, 3FH, 1EH, OOH, OOH
Text A:	Byte	7CH, 7EH, 13H, 13H, 7EH, 7CH, OOH, OOH
Text B:	Byte	41H, 7FH, 7FH, 49H, 49H, 7FH, 36H, OOH
Text C:	Byte	1CH, 3EH, 63H, 41H, 41H, 63H, 22H, OOH
Text D:	Byte	41H, 7FH, 7FH, 41H, 63H, 3EH,1CH, OOH
Text E:	Byte	41H, 7FH, 7FH, 49H, 5DH, 41H, 63H, OOH
Text F:	Byte	41H, 7FH, 7FH, 49H,1DH, 01H, 03H, OOH
Text G:	Byte	1CH, 3EH, 63H, 41H, 51H, 73H, 72H, OOH
Text H:	Byte	7FH, 7FH, 08H, 08H, 7FH, 7FH, OOH, OOH
Text I:	Byte	OOH, 41H, 7FH, 7FH, 41H, OOH, OOH, OOH
Text J:	Byte	30H, 70H, 40H, 41H, 7FH, 3FH, 01H, OOH
Text K:	Byte	41H, 7FH, 7FH, 08H, 1CH, 77H, 63H, OOH
Text L:	Byte	41H, 7FH, 7FH, 41H, 40H, 60H, 70H, OOH
Text M	Byte	7FH, 7FH, OEH, 1CH, OEH, 7FH, 7FH, OOH
Text N:	Byte	7FH, 7FH, 06H, OCH,18H, 7FH, 7FH, OOH
Text 0:	Byte	1CH, 3EH, 63H, 41H, 63H, 3EH,1CH, OOH
Text P:	Byte	41H, 7FH, 7FH, 49H, O9H, OFH, 06H, OOH
Text Q:	Byte	1EH, 3FH, 21H, 71H, 7FH, 5EH, OOH, OOH
Text R:	Byte	41H, 7FH, 7FH, O9H,19H, 7FH, 66H, OOH
Text S:	Byte	26H, 6FH, 4DH, 59H, 73H, 32H, OOH, OOH
Text T:	Byte	03H, 41H, 7FH, 7FH, 41H, 03H, OOH, OOH
Text U:	Byte	3FH, 7FH, 40H, 40H, 7FH, 3FH, OOH, OOH
Text V:	Byte	1FH, 3FH, 60H, 60H, 3FH,1FH, OOH, OOH
Text W:	Byte	7FH, 7FH, 30H, 18H, 30H, 7FH, 7FH, OOH
Text X:	Byte	43H, 67H, 3CH,18H, 3CH, 67H, 43H, OOH
Text Y:	Byte	07H, 4FH, 78H, 78H, 4FH, 07H, OOH, OOH
Text Z:	Byte	47H, 63H, 71H, 59H, 4DH, 67H, 73H, OOH

G1216 ADDRESSING LAYOUT (128 X 64)



G1213 ADDRESSING LAYOUT (128 X 32)



TERMINAL FUNCTIONS

Signal	Qty	I/O	Destination	Functions
DB_0 to DB_7	8	I/O	MPU	Common terminal for tristate input and output, and data bus. DB_7 = MSB
E	1	Input	MPU	Enable Write (R/W = 0): Latches data of DB_0 to DB_7 at the fall of E. Read (R/W = 1): Outputs data to DB_0 to DB_7 while "E" keeps a high level.
R/W	1	Input	MPU	Read/Write selection R/W = 1: When E = 1 and CS1 = O or CS2 = O, the data is output to DB_0 to DB_7 and read is available by MPU. R/W = 0: When CS1 = O or CS2 = 0, DB_0 to DB_7 are ready for receiving the input.
D/I	1	Input	MPU	Data Instruction selection D/I = 1: Indicates that the data in DB_0 to DB_7 is the display data. D/I = 0: Indicates that the data in DB_0 to DB_7 is the instruction code.
CS1, CS2	2	Input	MPU	Chip select input Active low. Data input and output is possible under the following status: LCM display screen CS1 | CS2 CS1: Controls the LCM left half display screen (SEG1 to SEG64). CS2: Controls the LCM right half display screen (SEG65 to SEG128).
RST	1	Input	MPU	Reset signal (Active low). Setting the RST signal to a low level allows for initial setup. (1) ON/OFF register: O setup (display OFF) (2) Display start line register: O line setup (display starts from O line) The setup status is retained until the status is changed by an instruction after reset is released.
V_{DD}	1	—	Power	Power terminal for logic (+5V)
V_{SS}	1	—	Power	GND terminal (OV)
V_{LC}	1	—	Power	Power terminal for LC drive
LEDA	1	—	Power	LED backlight anode terminal (+)
LEDC	1	—	Power	LED backlight cathode terminal (-)
F_{GND}	1	—	—	Frame ground[1]

[1] F_{GND} terminal is connected to the metallic frame of the module. Use this terminal when grounding the frame.

RESET FUNCTION

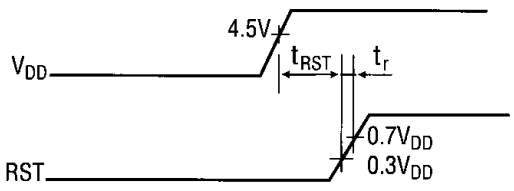
Setting the RST terminal to a low level when the power is on allows for initial setup.

1 Display OFF
2 Display start line register:
Set address 0. (G1213, G1216)
3. Address count mode: Up mode

G1213 & G1216: While the RST remains at a low level, instructions other than the Status Read cannot be accepted. Execute other instructions after confirming that DB4 = 0 (reset release) and DB7 = 0 (ready), using the Status Read instruction.

The power conditions for power-on initial setup are as follows:

Item	Symbol	Min.	Typ .	Max	Unit
Reset time	t_{RST}	1.0	—	—	μs
Rise time	t_R	—	—	200	ns

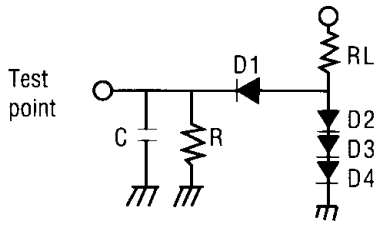


If the RESET is executed during operation, retention of the contents of all registers (excluding an ON/OFF register) and the RAM is not guaranteed. Always set them again.

TIMING CHARACTERISTICS

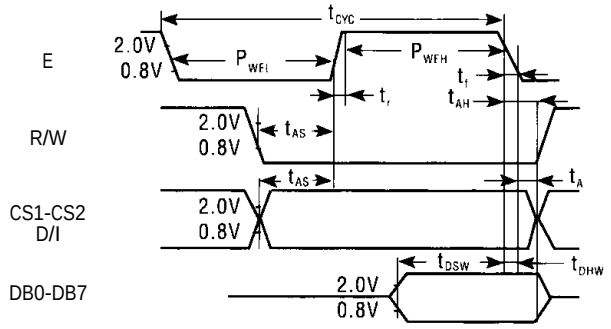
Item	Symbol	Min.	Typ.	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	1, 2
E high level width	P_{WEH}	450	-	-	ns	1, 2
E low level width	P_{WEL}	450	-	-	ns	1, 2
E rise time	t_r	-	-	25	ns	1, 2
E fall time	t_f	-	-	25	ns	1, 2
Address setup time	t_{AS}	140	-	-	ns	1, 2
Address hold time	t_{AH}	10	-	-	ns	1, 2
Data setup time	t_{DSW}	200	-	-	ns	1
Data delay time	t_{DDR}	-	-	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	-	-	ns	1
Data hold time (Read)	t_{DHR}	20	-	-	ns	2

DB0-DB7: LOAD CIRCUIT



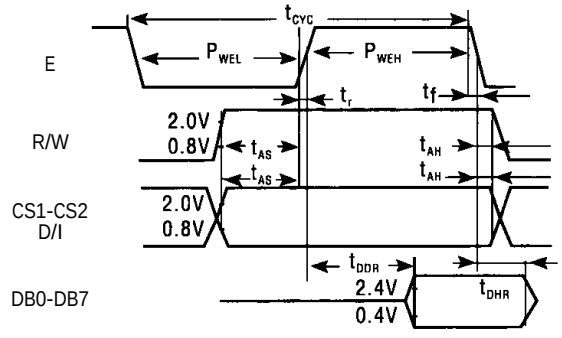
RL=2.4KΩ
R=11 KΩ
C=130pF (including jig capacity)
Diodes D1 to D4 are all 1S2074 (H).

DATA WRITE FROM MPU TO MODULE



CPU Write Timing

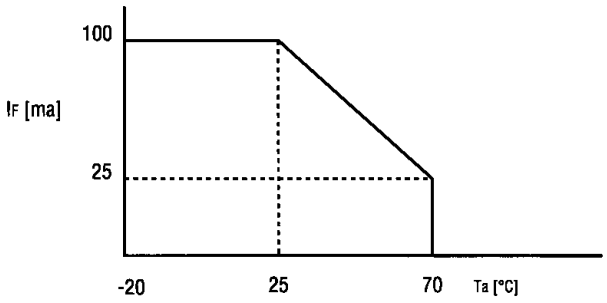
DATA READ FROM MODULE TO MPU



CPU Read Timing

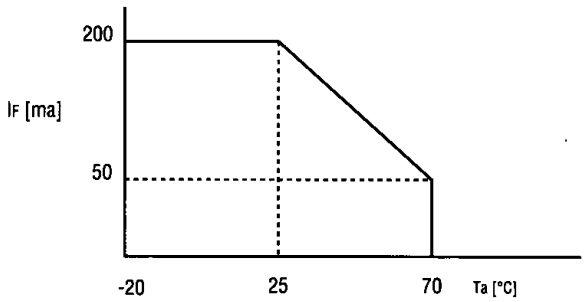
LED BACKLIGHT

G1213B1NOOO MAXIMUM RATING (12 LEDS)



Recommended LED current = 50 mA @ 25°C
Typical forward voltage = 4.1 VDC
Use 18 OHM current limiting resistor to + 5 VDC supply (PIN 19)

G1216B1N000
MAXIMUM RATING (20 LEDS)



Recommended LED current= 100 mA @ 25°C
Typical forward voltage = 4.1 VDC
Use 9.1 OHM current limiting resistor to + 5 VDC supply (PIN 19)

EXAMPLE OF CONNECTION TO Z80 MICROPROCESSOR